EC45

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NEW SCHEME

Fourth Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EC / EE / TE / IT / ML
Microprocessors

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. What is the difference between a microprocessor, a microcomputer and a microcontroller? **(06 Marks)**

b. What are memory, addressable memory, primary memory and memory map of a MP based system? How many address lines are required to address a memory of 16 KB? **(06 Marks)**

c. Draw the functional diagram used to explain the architecture of 8085 A microprocessor and mention the function of each part. **(08 Marks)**

2 a. Explain the function of the signal at each of the following pins of 8085 A : ALE ; READY ; and IO / M. **(06 Marks)**

b. List all the registers available in 8085 A microprocessor and state whether they are accessible or not in each case. What is the function of each of the inaccessible registers? **(06 Marks)**

c. Indicating the flag conditions, explain the operational difference between the following pairs of instructions :
   i) CALL 6644H and JMP 6644H;
   ii) SUB C and CMP C;
   iii) XRA A and MVI A 00H; and
   iv) SPHL and XTHL. **(08 Marks)**

3 a. Define instruction and instruction set. What are the fields of an instruction and what are the different ways of specifying these fields? **(06 Marks)**

b. What are loops and nested loops? Register C with an initial value of 55H is used as counter in a loop of a program. How many times will register C is decremented and how many times will the 'jump' takes place before exciting the loop? What is to be changed to make the program to loop 100 times? **(06 Marks)**

c. Define T-state, machine cycle and the instruction cycle. Draw the timing diagram for the instruction MVI A, 66H which is stored in memory starting from the address 5678H, indicating all the relevant contents given that the opcode for MVI A is 3E. **(08 Marks)**

4 a. What is stack memory? How is it initialized? Give the contents of SP register, register pairs and stack memory when each of the following instructions is executed. LXI SP, 8888H; LXI B, 11AA; LXI D, 22BB; LXI H, 33CC; PUSH B; PUSH D; PUSH H; .....; POP H; POP B; POP D; ..... **(06 Marks)**

b. Write an ALP to add N 8-bit numbers stored in the memory starting from the address 6650H. Store the result at 6690H and 6681H. **(06 Marks)**

c. Write an ALP to control a traffic signal, which turns on green light for 40 seconds, yellow light for 5 seconds and red light for 30 seconds. The bits 0, 1 and 2 of PORT 1 are controlling the peripherals that run the green, yellow and red signal light circuits respectively. Use an available 1 second DE register pair delay subroutine "DELAY". **(08 Marks)**

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5 a. What is subroutine? Why and how is it documented? Differentiate among nested subroutine; recursive subroutine; and multiple end subroutines. **(06 Marks)**

b. Write an ALP to clear all flags; load the data byte FFH into A Reg; increment the accumulator; mask all the flags except the carry flag; and display the carry flag at PORT 0. Again load the data byte FFH into A Reg; add the data byte 01H to it; mask all the flags except the carry flag; and display the carry flag at PORT 1. Explain the difference in the answer. **(06 Marks)**

c. Write an ALP to convert a given BCD number to an equivalent binary number. **(08 Marks)**

6 a. Differentiate between :
   i) Synchronous and Asynchronous data transfer;
   ii) Serial and Parallel data transfer;
   iii) Memory mapped I/O and I/O mapped I/O schemes. **(06 Marks)**

b. Explain the use of RIM and SIM instructions. How to mask RST7.5 and RST6.5 and to enable RST5.5 using SIM instruction? **(06 Marks)**

c. What are interrupts? How are they classified? Draw the diagram describing the interrupt structure of 8085A microprocessor. How is the address of the service routine resolved for nonvectored interrupts? **(08 Marks)**

7 a. Is it possible to interface an input device and output device with the same device address? If so, what control signals will differentiate these operations? Explain the reason for decoding the higher order address lines in interfacing an I/O device. **(06 Marks)**

b. Explain the terms :
   i) Linear-select decoding;
   ii) Absolute decoding; and
   iii) Bus contention. **(06 Marks)**

c. Draw an interfacing scheme for 2K ROM, 2KRAM, one input device and one output device using memory mapped I/O scheme. **(08 Marks)**

8 a. Explain the port selection logic and the control word format for different mode selection in 8255A PPI. **(06 Marks)**

b. What are the six modes of operation of 8253A programmable interval timer? Explain the control word format and mode definitions. **(06 Marks)**

c. What are the main functions of 8251A USART? Explain the mode instruction format and command instruction format for synchronous operation. **(08 Marks)**

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